

## Remarks

Claims 1-81 are currently pending in the Application. Claims 3, 7-11, 14-17, 19-22, 25, 29-33, 36-39, 41-44, 47, 51-55, 58-61, 63, 73-77 and 82-85 are withdrawn. Claims 12, 34, 56 are cancelled. Claims 1, 2, 4-6, 13, 18, 23, 24, 26-28, 35, 40, 45, 46, 48-50, 57, 62, 64-72 and 78-81 are rejected.

Claims 1, 23, 45, 67 and 78 are amended to include the limitation that a “0” is indicated by the complete absence of the carrier. Support for this amendment may be found at least on page 11, lines 12 to 14 and in figure 5.

**NFOA #2 Claims 1, 2, 4, 18, 23, 24, 26, 40, 45, 46, 48, 62, 64 and 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walker (US20020110190) in view of Vercellotti (US4653073).**

The Examiner relies on Walker to describe a communications system comprising a transmitter and receiver. Vercellotti is used to show the counting of cycles to indicate a “1” and a “0”. Applicant has amended claim 1 to require “the absence of ~~a specified number of all~~ cycles in said at least one digitally gated carrier wave indicates a second state of said digital data” as described in the specification page 11 lines 12 to 14 and shown in figure 5.

Vercellotti no longer describes applicant’s invention because Vercellotti teaches “If the input frequency is correct and maintains phase coherence for at least three fourths of the 1/6<sup>th</sup> bit interval, a counter is incremented. After six of these 1-6<sup>th</sup> bit intervals are processed, the counter contents are examined. If the counter counts up to four or more (assuming that it started out a 0), the demodulator outputs a demodulated logic 1. If the counter contents are less than 4, the demodulator outputs a demodulated logic 0.” (col 36 lines 34:42). By its own description, if Vercellotti’s demodulator 150 sees no carrier signal at all, it will not detect the correct frequency, and the phase coherence will not be satisfied for at least three fourths of the 1/6<sup>th</sup> bit intervals. As a result, demodulator 150 will not detect the passage of six 1/6<sup>th</sup> bit intervals and will not examine the counters for a one or zero. Hence the absence of all cycles during a “0” transmission means

Vercellotti's demodulator 150 will not increment and the presence of the logical "0" will be missed, counter to applicant's amended claim 1.

Since each and every claimed limitation is not found or suggested in the references singly or in combination as required by MPEP 2143.03 (citing *In Re Royka* 490 F.2d 981), the prima facie case of obviousness has not been made.

The Examiner may suggest some substitution or teaching, suggestion or motivation to use Vercellotti in Applicant's invention but that will require modification of Vercellotti's demodulator that results in the demodulator no longer performing its intended function. Moreover, there is no reasonable expectation of success for the modification in Vercellotti or Walker.

Applicant respectfully requests allowance of all claims.

#### Regarding Claims 2, 4 and 18

Claim 2 is allowable at least in that parent independent claim 1 is allowable.

Claim 4 requires in part "a digital gating device coupled to said carrier wave generator and controlled by said digital data, said digital gating device gating a carrier wave from said carrier wave generator on and off according to a state of the digital data." The Examiner points to Walker's paragraph 21 and 54 to support the gating of the carrier wave by the digital data. Yet Walker's paragraph 21 discusses "phase reversal keying a carrier frequency of a signal used for transmitting" not "gating a carrier wave from said carrier wave generator on and off according to a state of the digital data." as required by claim 4, Walker's paragraph 54 does not support the Examiner's either since figure 2 discussed in paragraph 54 does not contain, nor does paragraph 54 discuss, a carrier wave. Figure 2 and paragraph 54 of Walker discuss using a clock to delay and gate the digital data, but not to gate the carrier wave by the digital data as required by claim 4.

Withdrawal of claim 4's rejection is requested since not all elements of the claimed invention are shown in the references.

Claims 4 and 18 are allowable at least in that parent independent claim 1 is allowable.

Regarding claim 23

Claim 23 has been amended to state “the absence of ~~a specified number of all~~ cycles in said at least one gated carrier wave indicates a second state of said digital data” as in claim 1 and is allowable for the same reasons as claim 1.

Regarding Claims 24, 26 and 40.

Claims 24, is allowable in that independent claim 23 is allowable.

Claim 26 is allowable for the same reasons claim 4 is allowable discussed above.

Claim 40 is allowable in that independent claim 23 is allowable.

Regarding claim 45.

Claim 45 has been amended to state “the absence of ~~a specified number of all~~ cycles in said at least one gated carrier wave indicates a second state of said digital data” as in claim 1 and is allowable for the same reasons as claim 1.

Regarding claims 46, 48, 62, 64 and 66.

Claims 46, 48, 62, 64 and 66 are allowable in that independent claim 45 is allowable.

**NFOA #3 Claims 5,27, and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walker (US20020110190) and Vercellotti (US4653073) in view of Yousefi et al (US6957078).**

Claims 5, 27 and 49 are allowable at least in part for the same reasons as corresponding independent claims 1, 23 and 45 are allowable.

**NFOA #4 Claims 6,28, and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walker (US20020110190), Vercellotti (US4653073)and Yousefi et al (US6957078) in view of Staszewski et al (US20020186782).**

Claims 6, 28 and 50 are allowable at least in part for the same reasons as corresponding independent claims 1, 23 and 45 are allowable.

**NFOA #5 Claims 13, 35, and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walker (US200201 10190) and Vercellotti (US4653073) in view of Mohindra (US6922555).**

Dependent claims 13, 35 and 57 are allowable at least in part for the same reasons as corresponding independent claims 1, 23 and 45 are allowable.

The Examiner cites Mohindra for the “digital signal processor” of claim 13. Yet Mohindra col 4 line 57 to col 5 line 8 and the equations describes the demodulator 11 in figure 1 with outputs a function of the change in carrier phase. Nothing in Mohindra shows or suggests a “*digital signal processor*” (*italics added*) as required by claim 13.

In view of the differences between claim 13 and the cited reference and the novelty of independent parent claims 1, the Applicant respectfully requests the rejection of claim 13 based on 35USC103(a) be withdrawn.

In view of the novelty of parent claim 13, the Applicant respectfully requests the rejection of dependent claims 35 and 57 based on 35USC103(a) be withdrawn.

**NFOA #6 Claim 65 is rejected under 35 U.S.C. 103(a) as being unpatentable over Walker (US20020110190) and Vercellotti (US4653073) in view of MacLellan et al (US6456668).**

In view of the novelty of parent claim 45, the Applicant respectfully requests the rejection of dependent claim 65 based on 35USC103(a) be withdrawn.

**NFOA #7 Claims 67, 70-72, 78, 80, and 81 are rejected under 35 U.S.C. 103(a) as being unpatentable over Luhman et al (US20040223557) in view of Ainsworth (US5245630) and Walker (US200201 10190).**

Claim 67 has been amended to state “the absence of ~~a specified number of~~ all cycles in said at least one digitally gated carrier signal indicates a second state of said digital data” as in claim 1 and is allowable for the same reasons as claim 1.

Regarding claims 70-72

Claims 70-72 are allowable at least in part for the same reasons as independent claim 67 is allowable.

Regarding claims 78

Claim 78 has been amended to state “the absence of ~~a specified number of~~ all cycles in said at least one digitally gated carrier signal indicates a second state of said digital data” as in claim 1 and is allowable for the same reasons as claim 1.

Regarding claims 80 and 81

Claims 80 and 81 are allowable at least in part for the same reasons as independent claim 78 is allowable.

**NFOA #8 Claims 68, 69, and 79 are rejected under 35 U.S.C. 103(a) as being unpatentable over Luhman et al (US20040223557), Walker (US200201 10190) and Ainsworth (US5245630) in view of Cheng (US4789838).**

Dependent claims 68, 69 and 79 are allowable at least in part for the same reasons as independent parent claims 67 and 78 are allowable

### Conclusion

In view of the Examiner's failure to establish a prima facie case of obviousness as described above, reconsideration and allowance of all claims not cancelled or withdrawn is respectfully requested.

The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account no. 50-3984. In particular, if this response is not timely filed, then the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136(a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 50-3984.

Respectfully submitted,

/George R. Rapacki /  
George R. Rapacki  
HRL Patent Counsel  
Reg. No. 60770  
HRL Laboratories, LLC  
3011 Malibu Canyon Road  
Malibu, CA 90265  
(310) 317-5823